REMARKS

This communication is responsive to Office Action of December 18, 2003 in which the following objections were raised: [3] The drawings were objected to under 37 CFR 1.83(a) as failing to show key features as described in the specification; [4-5] Claims 1-10 and 12-19 are rejected under 35 U.S.C. 112 first paragraph as failing to comply with the enablement requirement; [6-7] Claims 1-10 and 12-19 are rejected under 35 U.S.C. 112 second paragraph as being indefinite; [8-9] Claims 1,3-4, 12 and 15 were rejected under 35 U.S.C. 102(e) as being anticipated by Timm et al. (U.S. 6,055,268); [10-11] Claims 2 and 13-14 were rejected under 35 U.S.C. 103(a) as being obvious over Timm et al. (U.S. 6,055,268), in view of Ali (Decimation-in-Time-Frequency FFT Algorithm"). [12] Claims 5-6, 9-10, and 18-19 are rejected under 35 U.S.C. 103(a) as being obvious over Timm et al. (U.S. 6,055,268) in view of Gossett et al. (U.S. 6,230,177); and [13] objections under 35 U.S.C. 132 to the amendment as adding new matter into the original disclosure.

Applicant has Amended Claims 1, 3, 5-10, 12, 14, 16-19 and added New Claims 22-23. The Applicant appreciates the Examiner's detailed Office Action.

AMENDMENTS TO THE SPECIFICATION:

Amendments to the portion of the specification pertaining to FIG. 12B, and FIGS. 13A-D have been made to correspond with the amendments to the corresponding drawings discussed below. Additionally the specification has been amended to conform the reference numbers in the specification with the reference numbers for the components of the deframer decoder 332 as shown in the originally filed FIG. 4.

AMENDMENTS TO THE DRAWINGS:

Applicant has amended FIG. 12B and FIGS. 13A-D. In the amended sheet FIG. 12B distinct reference numbers 1262-1264 have been given to the column transforms, replacing the former reference numbers 1252-1254. In FIGS. 13A-D the reference number used to reference the row and column transform component, and the reference numbers used to reference the input and output memories coupled thereto, have been amended to correct

obvious inconsistencies between the reference numbers used to refer to these components in the subject figures and in FIG. 4 in which they were initially introduced.

1-2. DRAWINGS OBJECTED TO UNDER 37 CFR 1.83(a) AS FAILING TO SHOW KEY FEATURES DESCRIBED IN SPECIFICATION :

The drawings were objected to under 37 CFR 1.83(a) as failing "*...to show key features as described in the specification*"... specifically: (a) two dimensional sample arrays each having dimensions corresponding with communication parameters of the associated one of the at least two communication channels (Claim 1) and (b) the number of tones exhibited by a first of the at least two communication channels differs from the number of tones exhibited by a second of the at least two communication channels (Claim 2). (Office Action of 12-18-03 at Page 2, Emphasis added).

The Applicant appreciates the telephonic conference with the Examiner on June 14, 2004 in which the Examiner and Applicant discussed 37 CFR 1.83(a), which reads in part:

> "*(a) The drawings in a nonprovisional application must show every feature of the invention specified in the claims....*" 37 CFR 1.83(a). (Emphasis Added by Applicant)

Applicant and Examiner appear to have divergent opinions on the interpretation of 37 CFR 1.83(a). The Applicant respectfully submits that either Amendments to the Claims to remove the objected to features or a recitation of support in the Drawings for the Claimed features without amendment to the Claims constitutes a proper response to this objection.

The Examiner appeared to prefer that the Applicant address the drawing objections irrespective of any amendment to the Claims. In the remainder of this section the drawing objection will therefore be addressed by a recitation of the support in the drawings for the features said to be lacking support therein by the Examiner on page 2 paragraph 3 of the Office Action of 12-18-2003.

The support in the drawings for the features:"... *'two dimensional sample arrays each having dimensions corresponding with communication parameters of the associated one of the at*

least two communication channels'... 'and 'the number of tones exhibited by a first of the at least two communication channels differs from the number of tones exhibited by a second of the at least two communication channels'... " (Office Action of 12-18-2003 at page 2, paragraph 3) is found in drawings as follows:

Data Structure Diagram(s): FIG. 11C is a data structure diagram showing the corresponding row and column dimensions of seven different two-dimensional sample arrays for DMT protocols shown in FIGS. 11A-B with differing number tones or sub-carriers and a differing number of samples, e.g. 4k,2k,1k,512,256, 128 and 64, per sample set. *"FIG. 11C shows row and column dimensions for transforms performed on various of the standard X-DSL sample sets within the FTE 322 shown in FIGS. 3-4."* (Specification at page 21, lines 22-24). *"... each device packet is correlated with a channel and protocol and mapped into input memory .... in a row and column order. ... the complex symbols are modulated into carriers or tones in the row and column transform component 414 and placed in either portion 410 or 412 of output memory. The dimensions of the row and column transforms vary on a channel specific basis as shown in the following FIG. 11C.* " (Specification at page 13, lines 18-23)

Data Flow Diagram(s): FIG. 8 is a data flow diagram showing the pipelined processing of successive sample sets 800, 804 from a first channel, Channel 1, and 802 from a second channel, Channel 2, which differ from one another in a number of samples per sample set. Channel 1 is shown with N_1-1 samples per sample set and Channel 2 with N_2-1 samples per sample set. *"Where multiple sample, e.g. 802 [Channel 2], 804[Channel 1] of varying sizes are pipelined through the FTE ...."* (Specification at page 16, lines 25-26, Bracketed portions reference the corresponding labels in the associated drawing).

Isometric Diagram(s): FIGS. 9AB are isometric diagrams of representative two-dimensional sample arrays with respectively 32 columns and 64 rows in FIG. 9A and with 64 columns and 64 rows in FIG. 9B. FIGS. 9AB and FIG. 10 show detailed isometric representations of the novel process of iterative partial row transforms followed by complete column transforms by which two dimensional processing of arrays of different sizes are handled in accordance with the current invention.

Hardware Block Diagram(s): FIGS. 13A-D, 14A-B and 15, show various detailed hardware block diagrams of an embodiment of the Fourier Transform Engine for high

throughput pipelined processing of sample arrays of varying domains, and varying numbers of samples per sample set.

Process Flow Diagram: FIG. 16 is a detailed process flow diagram of an embodiment of the processes of the current invention as executed in a Fourier Transform Engine implemented in accordance with the current invention implemented in a digital signal processor (DSP). The discrete Fourier transform (DFT) processes include the following acts:

"Processing begins after initialization 1600 in process 1602 in which a packet containing the sample set corresponding with the next channel is input into memory. In process 1604 the protocol associated with the channel is determined. Control is then passed to decision block 1606 in which a determination is made as to the transform to be performed, e.g. DFT/IDFT. This determination may be made directly on the basis of the header on the incoming packet, or the state of the switch 420 which couples the upstream and downstream path to input memories 416-418. Next in process 1648 the sample size is determined based on the indicia in the device packet header. This determination may be made directly as a result of information in the header, or indirectly by correlating the channel identifier in the header with the parameters stored for the channel in main memory 326 or the component register during session setup. (See FIG. 4). Once the sample size is determined the row and column transform parameters (See FIG. 11C) are used to configure the RC component 414 (See FIG. 4)." (Specification at page 26, lines 16-26, Emphasis Added). *"If alternately, in decision process 1606 a determination is made that the transform to be performed is an IDFT then control passes to process 1608 in which the sample size is determined based on the indicia in the device packet header. Once the sample size is determined the row and column transform parameters (See FIG. 11C) are used to configure the RC component 414 (See FIG. 4). Next in process 1610 the input sample set is mapped into a first two dimensional array 850 (See FIG. 9B)."* (Specification at page 27, lines 18-22, Emphasis Added).

The Applicant respectfully submits that the drawings provide multiple views in a variety of drawing formats including: data structure, data flow, isometric, hardware block, and process flow of the above referenced features. Given the above referenced support in the drawings for the stated features the Applicant respectfully requests that this rejection has been overcome and that the Examiner withdraw the rejection.

4-5. CLAIMS 1-10 AND 12-19 REJECTED UNDER 35 U.S.C. 112 1ST PARAGRAPH:

Claims 1-10 and 12-19 are rejected under 35 U.S.C. 112 first paragraph as failing to comply with the enablement requirement in particular: (a) two dimensional sample arrays each having dimensions corresponding with communication parameters of the associated one of the at least two communication channels; (b) device packets encapsulating each sample array and each device packet identifying both the corresponding one of the at least two communication channels; (c) the number of tones exhibited by a first of the at least two communication channels differs from the number of tones exhibited by a second of the at least two communication channels; (d) at least one variable order radix sub-module responsive to the input of each sample array to vary an order of the radix based on the dimensions of the sample array; and (e) logic for reducing the dimensions of sample arrays which exhibit hermetian symmetry by excluding any mirror reversed conjugates there from. (Office Action of 12-18-03 at Page 3).

Applicant has Amended all Claims rejected under 35 USC 112 first paragraph and has cancelled Claims 2, 4, 13, and 15. Following the approach used in the drawing rejections, and as also discussed with the Examiner in a second TPC on June 14, 2004 the objection will be addressed by a lengthy, though not necessarily exhaustive, recitation of the portions of the specification in which a written description of the objected to subject matter is found.

The support in the specification for the objected to subject matter is as follows:

(a) two dimensional sample arrays having variable dimensions corresponding with communication parameters of the associated one of at least two communication channels...:

FIGS. 1-3 and the accompanying description in the Specification set forth an embodiment of the invention in which a single DSP 218 (See FIG. 2) handles multiple communication channels each modulated in different X-DSL protocols. *"On these subscriber lines voice band and data communication are provided. The data communication is shown as various X-DSL protocols including G.Lite, ADSL VDSL, and HDSL2. CO 100 is coupled via G.Lite and ADSL modulated subscriber line connections 160 with subscribers 110 and 112. CO 100*

is also coupled via G.Lite and ADSL modulated subscriber line connections 162 with subscriber 114. CO 106 is also coupled via a subscriber line to subscriber 134. Remote access terminal is coupled via subscriber line connections 164 with subscribers 120. In each case the corresponding CO may advantageously be provided with distributed AFE and DSP resources for handling multiple protocols from multiple locations with the added benefit of load balancing, and statistical multiplexing." (Specification page 6, lines 19-28). *"The input controller 330 handles the mapping of data and the processing of the packets as it flows through FTE. The information in the header of the packet is used by the controller 330 to maintain the channel identity of the data as it is demodulated, to setup the FTE at the appropriate parameters for that channel, e.g. sample size, and to provide channel specific instructions for the demodulation of the data."* (Specification at page 9, lines 3-6)

A complete and self-sufficient mathematical exposition of both DFT and IDFT processing in accordance with an embodiment of the invention is set forth under the portion of the specification sub-titled "**The two dimensional DFT/IDFT**" An example for a sample set of 4k samples per set is set forth. (Specification at page 17, line 1 through page 19, line 19).

FIG. 4 and the accompanying description set forth a detailed embodiment of the invention in which multiple AFE's 212-214 each supporting multiple subscriber lines are coupled to a single DSP 218 for processing. *"...[S]uccessive downstream packets carry downstream channels each of which implements different protocols, e.g. G.Lite, ADSL, and VDSL the sample rate of the analog mux 384 the filter parameters for the corresponding filter 390 and the gain of the corresponding analog amplifiers 394 will vary for each packet. This "on the fly" configurability allows a single downstream pipeline to be used for multiple concurrent protocols.* "(Specification at page 10, lines 28-34) *"The tone orderer [442] supports varying number of tones, bytes per tone and gain per tone for each of the X-DSL protocols. For example the number of tones for G.Lite is 128, for ADSL is 256 and for VDSL 2048. The number of bits to be extracted per tone is read from the tone-ordering table or register at the initiation of processing of each packet. For example as successive packets from channels implementing G.Lite, ADSL and VDSL pass through the DMT Tx engine the number of tones*

will vary from 128 for G.lite, to 256 for ADSL, to 2048 for VDSL. " (Specification at page 13, lines 9-16).

FIG. 4 also shows the DFT 424 and IDFT 422 mappers which in an embodiment of the invention handle the writing of each sample set into memory into a corresponding two-dimensional array having row and column dimensions corresponding with the communication parameters of the channel, e.g. the number of samples per sample set. " *The DFT mapper is coupled to the input memory portion of the FTE via a multiplexer 420. The mapper handles writing of each sample set from a packet into the input memory in the appropriate order.*" (Specification at page 11, lines 26-27) "*Next in the IDFT mapper each device packet is correlated with a channel and protocol and mapped into input memory via a connection provided by multiplexer 420. The mapping is in a row and column order.* "(Specification at page 13, lines 18-20) "*The control of the writing to memories is accomplished by a mapper 1010 corresponding with either of the IDFT or DFT mappers 422-424 respectively (See FIG. 4).*" (Specification at page 21, lines 15-18).

FIG. 11C and the accompanying description show the corresponding row and column dimensions of seven different two-dimensional sample arrays for DMT protocols shown in FIGS. 11A-B with differing number tones or sub-carriers and a differing number of samples, e.g. 4k,2k,1k,512,256, 128 and 64, per sample set. "*FIG. 11C shows row and column dimensions for transforms performed on various of the standard X-DSL sample sets within the FTE 322 shown in FIGS. 3-4.*" (Specification at page 21, lines 22-24). "*... each device packet is correlated with a channel and protocol and mapped into input memory .... in a row and column order. ... the complex symbols are modulated into carriers or tones in the row and column transform component 414 and placed in either portion 410 or 412 of output memory. The dimensions of the row and column transforms vary on a channel specific basis as shown in the following FIG. 11C.* " (Specification at page 13, lines 18-23)

FIG. 8 and the accompanying description show the pipelined processing of successive sample sets 800, 804 from a first channel, Channel 1, and 802 from a second channel, Channel 2, which differ from one another in a number of samples per sample set. Channel 1 is shown

with N_1-1 samples per sample set and Channel 2 with N_2-1 samples per sample set. *"Where multiple sample, e.g. 802 [Channel 2], 804[Channel 1] of varying sizes are pipelined through the FTE ...."* (Specification at page 16, lines 25-26, Bracketed portions reference the corresponding labels in the associated drawing).

FIG. 16 and the accompanying description show an embodiment of the processes of the current invention as executed in a Fourier Transform Engine implemented in accordance with an embodiment of the current invention implemented in a digital signal processor (DSP). The discrete Fourier transform (DFT) processes include the following acts: *"Processing begins after initialization 1600 in process 1602 in which a packet containing the sample set corresponding with the next channel is input into memory. In process 1604 the protocol associated with the channel is determined. Control is then passed to decision block 1606 in which a determination is made as to the transform to be performed, e.g. DFT/IDFT. This determination may be made directly on the basis of the header on the incoming packet, or the state of the switch 420 which couples the upstream and downstream path to input memories 416-418. Next in process 1648 the sample size is determined based on the indicia in the device packet header. This determination may be made directly as a result of information in the header, or indirectly by correlating the channel identifier in the header with the parameters stored for the channel in main memory 326 or the component register during session setup. (See FIG. 4). Once the sample size is determined the row and column transform parameters (See FIG. 11C) are used to configure the RC component 414 (See FIG. 4)."* (Specification at page 26, lines 16-26, Emphasis Added). *"If alternately, in decision process 1606 a determination is made that the transform to be performed is an IDFT then control passes to process 1608 in which the sample size is determined based on the indicia in the device packet header. Once the sample size is determined the row and column transform parameters (See FIG. 11C) are used to configure the RC component 414 (See FIG. 4). Next in process 1610 the input sample set is mapped into a first two dimensional array 850 (See FIG. 9B)."* (Specification at page 27, lines 18-22, Emphasis Added).

(b) device packets encapsulating each sample array and identifying .....channels:

The DSP device packets 306 and the processing of same are described in FIG. 3-4 and the accompanying specification. FIG. 5 and the accompanying specification offer a detailed description of an embodiment of a DSP device packet. " *The operation of the DSP PAD for upstream packets is managed by controller 318. For upstream packets, the PAD handles removal of the DSP bus packet header and insertion of the device header and control header which is part of the device packet 306. (See FIG. 5). The content of these headers is generated by the core processor 334 using information downloaded from the DSLAM controller 200 (See FIG. 2) as well as statistics such as gain tables gathered by the de-framer 332, or embedded operations channel communications from the subscriber side. These channel specific and control parameters 326 are stored in memory 328 which is coupled to the core processor. The PAD 316 embeds the required commands generated by the core processor in the header or control portions of the device packet header of the upstream data packets. The upstream packets may collectively include data from multiple channels each implementing various of the X-DSL protocols. Thus the header of each device packet identifies the channel corresponding with the data contained therein. Additionally, a control portion of the packet may include specific control instructions for any of the discrete or shared components which make up the upstream or downstream processing paths. In the embodiment shown, the Fourier transform engine (FTE) 322 is a component which is shared between the upstream and downstream paths. Thus, on the upstream path each upstream packet is delivered to the FTE for demodulation. The input controller 330 handles the mapping of data and the processing of the packets as it flows through FTE. The information in the header of the packet is used by the controller 330 to maintain the channel identity of the data as it is demodulated, to setup the FTE at the appropriate parameters for that channel, e.g. sample size, and to provide channel specific instructions for the demodulation of the data. The demodulated data is passed under the control of output controller 324 as a packet to the next component in the upstream path, i.e. the deframer and Reed Solomon decoder 332 for further processing. This component reads the next device packet and processes the data in it in accordance with the instructions or parameters in its header. The demodulated, decoded and de-framed data is passed to the asynchronous transfer mode (ATM) PAD 340 operating under the control of controller 338. In the ATM PAD the device packet header is removed and the demodulated data contained therein is wrapped with an*

ATM header. The packet is then passed to the ATM MAC 344 for transmission of the ATM packet on the ATM network 140 (See FIGS. 1-2).

On the downstream path, downstream packets containing digital data destined for various subscribers is received by the ATM MAC 344 which handles transfers to and from the ATM network 140. The ATM MAC passes each received packet to the ATM PAD 340 where the ATM header is removed and the downstream device packet 306 is assembled. The operation of the ATM PAD for downstream packets is managed by controller 342. Using header content generated by the core processor 334 the PAD assemble data from the ATM network into channel specific packets each with their own header, data and control portions. The downstream packets are then passed to the Framer and Reed Solomon encoder 336 where they are processed in a manner consistent with the control and header information contained therein. The Framer downstream packets are then passed to the input of the FTE. The control 330 governs the multiplexing of these downstream packets which will be modulated by the FTE with the upstream packets which will be demodulated therein. Each downstream packet with the modulated data contained therein is then passed to the DSP PAD." (Specification at page 8, line 17 through page 9 line 27, Emphasis added).

"The mapper handles writing of each sample set from a packet into the input memory in the appropriate order." (Specification at page 11, lines 26-27). "When a change in gain table for a particular channel is called for the core processor sends instructions regarding the change in the header of the device packet for that channel via PAD 316." (Specification at page 12,lines 23-26). *"The number of bits to be extracted per tone is read from the tone-ordering table or register at the initiation of processing of each packet."* (Specification at page 13, lines 11-12). *"This device architecture allows the DSP transmit and receive paths to be fabricated as independent modules or submodules which respond to packet header and or control information for processing of successive packets with different X-DSL protocols, e.g. a packet with ADSL sample data followed by a packet with VDSL sampled data. A mixture of different control techniques are used to control the behavior of the individual components of the DSP. The packet header may simply identify the channel. The component receiving the packet may then reference internal registers or downloaded tables such as table 326 to correlate the channel with a protocol and the protocol with the corresponding parameters with which the data portion of the packet is to be processed. Alternately the*

device packet may contain specific control information such as that associated with shutting down a channel, idling a channel, or shutting down the DSP. "(Specification at page 14, lines 1-11, Emphasis added).

"FIG. 5 shows the device packet structure for passing data through and controlling the operation of various components within the DSP shown in FIG. 4. The device packets each include a header portion 308, a command portion 310 and a payload or data portion 312. In an embodiment of the invention the header is of a fixed length. The header in this embodiment of the invention includes five fields. Field 520 contains a value corresponding with the size of the packet. Field 526 identifies the channel associated with the packet. Field 528 indicates any common operations among modules to be performed on a channel, i.e. active, inactive, idle etc. Field 522 contains flags for each module in the associated path, i.e. transmit or receive, and a command size field 524. The command portion 310 may contain no command blocks or may contain command blocks for one or more of the modules or components on the transmit/receive path. Three command blocks 530, 532, 534 are shown.

The core processor 334 (See FIGS. 3-4) "talks" to selected modules indirectly through these packets and specifically via either the common ops field 528 or the command fields 520-524 thereof. When the core processor has scheduling, setup, changeover, timing or other information for a selected module it passes the information to the module indirectly via headers for the associated channel together with the appropriate module. Thus the behavior of individual modules may be configured on the fly on a channel by channel basis.

As each module receives each packet it performs two operations on the header. An update of the packet data size is performed on every packet when the processes performed by the module, e.g. DFT or IDFT change the size of the payload. The module updates the value in field 320 with the new packet size. The other operation is only performed when the module/component receives a device packet in which its, the modules, unique flag bit in field 522 is set. If its flag bit is set, the module reads data starting from the start of the command portion 310 in an amount corresponding with the command size indicated in field 524. If the command is one to be executed on the current payload then the receiving module makes the changes and processes the payload data 534. If the command sequence is to be performed on

a subsequent packet then the module logs the command and frame reference and executes it at the appropriate frame. After reading the command and processing the data, and before transferring the processed device packet to the next module in the queue the detecting module performs the following operations. It deletes its command information effectively by writing the packet out with the succeeding command blocks 532-534 moved from the second and third positions to the first and second positions within the command portion (See detailed views). Then the component updates both the command size in the command size field 524 as well as the packet data size 520." (Specification at page 14, line 12 through page 15, line 13, Emphasis added).

"*FIG. 6 is a process flow diagram showing the operation of various shared and dedicated components within the DSP in response to the receipt of upstream or downstream device packets 306. Each of the shared and dedicated components/modules responds to header and control information in the device packets to reconfigure its process parameters for processing of the data portion 312 of the device packet. Device packets may in alternate embodiments of the invention be implemented on either the DSP or the AFE should timing, scheduling, scalability etc. make it advantageous to do so. Processing begins in start bock 600 in which control is passed to process 602 for the receipt of the next packet. Next in process 604 the common ops field 528 (See FIG. 5) is read to see if there are any common ops in the header to be executed. Common ops include a state change for a channel, e.g. active-> inactive/idle. Then in process 606 the command bit in command flag field 522 is read. If in decision process 608 a determination is made that the flag bit for the corresponding module is not set then that module executes process 632. In process 632 the device packet is processed using parameters previously associated with the channel in main memory 328 (See FIGS. 3-4) or in a memory/register associated with the component. These parameters may be downloaded or fixed part of memory. Next the module updates the header with the new data size in field 520 and passes the packet to the next submodule, module or FIFO buffer. Alternately, if in decision process 608 a determination is made that the flag bit for the module is set, then control is passed to process 610 in which the command is read. Control then passes to processes 614-618. In process 614 the command is acted on or stored for action on a later packet. This later feature permits synchronization with other modules. Next in process 616 the command for the component is deleted from the command*

block and any remaining commands re-written, e.g. moved forward in the command portion 310. Then in process 618 the updated device packet with processed data and updated header information, e.g. packet size, is assembled and passed to the next component. This approach has the advantage of avoiding detailed timing, synchronization and control of the individual modules. Each component may be individually configured using either in packet or out of packet control techniques. " (Specification at page 15 line 14 through page 16, line 8).

In FIG. 16 and the accompanying description the processes associated with handling of device packets in the Fourier Transform Engine are set forth in part as follows: "*Next in process 1648 the sample size is determined based on the indicia in the device packet header. This determination may be made directly as a result of information in the header, or indirectly by correlating the channel identifier in the header with the parameters stored for the channel in main memory 326 or the component register during session setup. (See FIG. 4).*" (Specification at page 26, line 22-23 and FIG. 16.).

(c) the number of tones exhibited by a first of the at least two communication channels differs from the number of tones exhibited by a second of the at least two communication channels...:

FIGS. 3-4 and the accompanying description show a single DSP 218 handling the modulation and demodulation of multiple communication channels each with distinctive X-DSL protocol differing in tones from one another. Subscribers 110, 112, 114 are shown coupled via corresponding subscriber lines to the CO 100 and specifically the DSP 218. Communications between subscriber 110 and the CO are conducted over the corresponding subscriber line using the G.Lite X-DSL protocol with 128 tones for Transmission and 32 tones for Reception (See FIG. 11A-B). Communications between subscriber 112 and the CO are conducted over the corresponding subscriber line using the ADSL X-DSL protocol with 256 tones for Transmission and 32 tones for Reception (See FIG. 11A-B). Communications between subscriber 114 and the CO are conducted over the corresponding subscriber line using the VDSL X-DSL protocol with the number of tones depending on the particular VDSL protocol implemented on the transmit and receive paths. (See FIG. 11A-B).

"*For example, where successive downstream packets carry downstream channels each of which implements different protocols, e.g. G.Lite, ADSL, and VDSL the sample rate of the analog mux 384 the filter parameters for the corresponding filter 390 and the gain of the corresponding analog amplifiers 394 will vary for each packet. This "on the fly" configurability allows a single downstream pipeline to be used for multiple concurrent protocols.*" (Specification at page 10, line 28-34, Emphasis added).

"*A multiplexer 430 couples the deframer input to either the tone reordered 428 or to the output memory of the FTE. Each of these components is individually configurable on a per channel basis using tables stored locally in registers within each component, or within memory 328. The access to these tables/registers is synchronized by the logic in each of the components which responds to header or control information in each upstream packet to alter tone ordering/re-ordering, gain scaling constants per-tone per-channel, and FEQ constants per-tone per-channel. The processor 334 may initialize all the registers.*"
(Specification at page 12, lines 11-19)

"*The tone orderer supports varying number of tones, bytes per tone and gain per tone for each of the X-DSL protocols. For example the number of tones for G.Lite is 128, for ADSL is 256 and for VDSL 2048. The number of bits to be extracted per tone is read from the tone-ordering table or register at the initiation of processing of each packet. For example as successive packets from channels implementing G.Lite, ADSL and VDSL pass through the DMT Tx engine the number of tones will vary from 128 for G.lite, to 256 for ADSL, to 2048 for VDSL. In the encoder 444 constellation mapping is performed based on the bit pattern of each packet. The output is a two dimensional signal constellation in the complex domain.*"
(Specification page 13, lines 9-17, Emphasis added)

(d) at least one variable order radix sub-module responsive to the input of each sample array to vary an order of the radix based on the dimensions of the sample array:

"*FIG. 13C shows the FTE configuration for an DFT. In the example shown the time domain sample set of all real values was compressed by half into an array of complex values. At the output a complex conjugator will be used to expand the column transform output of frequency domain coefficients back to the size of the original sample. The sliced radix circuit discussed*

above provides the first processing stage of the RC engine. The sliced radix circuit has 4 parallel inputs generally 1390 which correspond in number with the order of the radix. Its output is coupled to the input of a remaining row portion 1310 of the row transform. In the example shown that module 1310 includes a variable order radix 1312 with an order variable between Rmax and Rmin. In the example shown Rmax = 16 and Rmin = 2. That variable order radix couples with the Twiddle factor generator 1314. The transformed output of the variable order radix is passed via switch 1316 to multiplier 1320. The multiplier multiplies twiddle factors from generator 1318 times the input and passes these via switch 1322 to either of RC memories 1326-1328.

The output from RC memory is passed to the first stage 1336 of two column transform stages 1336-1338. In the first stage a radix "R" 1352 and associated twiddle driver 1360 provides an output to multiplier 1354. The output is scaled by the multiplier with a twiddle factor 1362 and the resultant is passed to the input of a variable order radix 1356 with an order also variable between Rmax and Rmin. In the example shown Rmax = 16 and Rmin = 2. That variable order radix couples with the associated twiddle factor generator 1364. The transformed output of the variable order radix is passed via switch 1358 to the second stage module 1338." (Specification at page 23, line 31 through page 24, line 19, Emphasis added)

" FIG. 15 is a hardware block diagram of an embodiment of a variable radix component 1312 (See FIG. 13) within the row and column component portions of the Fourier transform engine 322 (See FIG. 3). The input to the circuit 1500 is switchably coupled into the cascade of fixed radix order "2" processors 1502, 1508, 1514, 1520 at a point at which the product of the radix orders corresponds with the size of the overall transform to be performed. Switches 1506, 1512, and 1518 couple the input line 1500 to respectively radix 1508, 1514, and 1516. Rotator 1504 couples the output of radix 1502 to the input of radix 1508 via switch 1506. Complex multiplier 1510 couples the output of radix 1508 to the input of radix 1514 via switch 1512. Rotator 1516 couples the output of radix 1514 to the input of radix 1520 via switch 1518. In alternate embodiments of the invention where sample sizes exceed 4k the range of configurability may be increased by extending the cascade." (Specification at page 26, lines 4-14, Emphasis added)

"The input controller 330 handles the mapping of data and the processing of the packets as it flows through FTE. The information in the header of the packet is used by the controller 330 to maintain the channel identity of the data as it is demodulated, to setup the FTE at the appropriate parameters for that channel, e.g. sample size, and to provide channel specific instructions for the demodulation of the data. " (Specification at page 9, line 1-6, Emphasis added)

(e) logic for reducing the dimensions of sample arrays which exhibit hermetian symmetry by excluding any mirror reversed conjugates there from:

"FIG. 9B shows similar processing for the IDFT. The set is mapped into input memory as an array of 64 columns and 64 rows. For the IDFT a 4k input sample with Hermetian symmetry is treated as a sample set 33 rows rather than 64 due to the property of the Hermetian which characterizes all rows 866 beyond one below the middle row to be characterized as complex conjugates of a corresponding row in the top half of the input array. If the inverse Fourier Transform results in real valued sequence then the resulting 2-D map has the following Hermetian symmetry: If we denote the elements of row i as $R_i(j)$ *where* $j = 0, \ldots, C\text{-}1$ *then:*

$$R_i(j) = R^*_{R-i}(C-j) \text{ for } i = 1, \ldots, R/2-1, R/2+1, \ldots R-1 .$$

Therefore $R_0(j)$ *has the same structure as the original sequence x(k) and* $R_{N/2}(j)$ *is a mirror reversed conjugate sequence with* $R_{N/2}(j) = R^*_{N/2}(C-j)$ *for* $j=0, \ldots, N/2-1$.

Thus a transform of the top half of the rows is followed by a conjugation operation to expand the number of rows output to RC memory back to their original value. No loss of accuracy and a considerable savings in time is a result of taking advantage of this special case, unique to DMT communication protocols." (Specification at page 20, lines 6-21, Emphasis added)

"FIG. 12B is a timing diagrams showing the timing associated with the row and column transforms of the IDFT. An input exhibiting hermetian symmetry is shown. The input array

of frequency domain samples 850 is folded into a two dimensional array with 64 columns and after removing the lower conjugates 866 has 33 rows remaining. Each row, e.g. row 870 of the array is subject to a sliced radix transform which results in a solution to a slice of the inner nested summation shown in Equation 2 above." (Specification at page 20, lines 6-21, Emphasis added)

"FIG. 13D shows the FTE configuration for an IDFT. In the example shown the frequency domain sample set which exhibits hermetian symmetry is subject to row reduction to avoid transforming rows which are merely complex conjugates. These rows will be regenerated after the row transformation. The sliced radix circuit discussed above provides the first processing stage of the RC engine. The sliced radix circuit has 4 parallel inputs generally 1390 which correspond in number with the order of the radix. Its output is coupled to the input of a remaining row portion 1310 of the row transform as discussed above in connection with the DFT circuit configuration. The processing of the row is substantially similar to that discussed above in FIG. 13C, with one exception, the output of the row transform is expanded by supplying both the direct output from switch 1322 and the conjugated output from conjugator 1324 to RC memory.

The output from RC memory is passed to the first stage 1336 of the column transform as discussed above in connection with the DMT. The output from the RC memory is also provided via switch 1332 to a second first stage module 1334 which performs similarly to the first albeit with different slices to compute (See FIG. 12B). The outputs of the first stage and the second first stage are supplied to output memory via switches 1382-1384 respectively. This real valued time domain coefficients are stored in either of output memories 412/410." (Specification at page 24, line 32 through page 25 line 15, Emphasis added).

FIG. 16 sets forth the processes for exploiting hermetian symmetry in an input sample set. *"If alternately, in decision process 1606 a determination is made that the transform to be performed is an IDFT then control passes to process 1608 in which the sample size is determined based on the indicia in the device packet header. Once the sample size is determined the row and column*

transform parameters (See FIG. 11C) are used to configure the RC component 414 (See FIG. 4). Next in process 1610 the input sample set is mapped into a first two dimensional array 850 (See FIG. 9B). Control is then passed to process 1612 in which the row count to be processed is reduced by the number of conjugates if the input frequency domain sample set exhibits hermetian symmetry. Control is then passed to process 1614 in which the complex output or slice of the sliced radix component at the input of the RC transform is set. Next in process 1616 the first row of the 2D input sample set array is fetched and in process 1618 it is folded/decomposed into a second 2D array with a number of columns equal to the order "R" of the sliced radix input to the RC transform. The parallel inputs of all rows in the second decomposed array are successively applied to the sliced radix input of the row transform in processes 1620-1626 during which the row and column transforms are applied to these inputs. During this process the row output is conjugated to recapture the rows for which the transform was avoided due to the hermetian symmetry in the input sample set. Then in processes 1628 the outputs of the column transforms are placed in output memory. In decision process 1630 this process is repeated with the fetching of the next row in the 1st 2D sample array in process 1616. This loop is repeated until the end of the rows in the 2nd 2D array at which point a determination is made in decision process 1630 as to whether another slice remains for the sliced radix input to take on the input sample 2D array. If so the row counter for the first 2D array is reset and the next slice scalar input is provided to the inputs of the sliced radix in process 1634, after which control returns to process 1616 for the fetching of the next row.

When the processing of all slices across all input rows is complete control passes from decision process 1632 to the transmit frame process 1636 in which the time domain coefficients are passed to the AFE for transmission to a subscriber. Subsequently control returns to process 1602 for the fetching or delivery of the next channel to the RC transform 414 (See FIG. 4)." (Specification at page 24, line 32 through page 25 line 15, Emphasis added).

The Applicant has Amended all Claims rejected under 35 USC 112 first paragraph and has cancelled Claims 2, 4, 13, and 15. The Applicant respectfully submits that the specification and drawings provide multiple overlapping views and descriptions of the rejected subject matter each of which individually and all of which collectively fully satisfy the written description requirement for at least the reasons stated above. Given the above

referenced support in the specification and drawings for that subject matter the Applicant respectfully requests that this rejection has been overcome and that the Examiner withdraw the rejection.

6-7. CLAIMS 1-10 AND 12-19 REJECTED UNDER 35 U.S.C. 112 2ND PARAGRAPH:

Claims 1-10 and 12-19 are rejected under 35 U.S.C. 112 second paragraph as being indefinite.

Applicant has Amended Claims 1, 3, 5-10, 12, 14, 16-19 and cancelled Claims 2, 4, 13, and 15.

Re Claim 1: Applicant's amendment to Claim 1 has removed the language said to be indefinite on lines 5-7 and 9. As the Examiner's rejection of the limitations in part b, the Applicant has further amended the claimed features of the Fourier transform circuit, and has broken out as sub-elements the row transform components and the column transform components to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

All remaining rejected Claims in this section have been extensively amended by the Applicant to overcome the Examiner's rejections, and the Applicant requests that the Examiner withdraw this rejection.

8-9. CLAIMS 1,3-4, 12 AND 15 REJECTED UNDER 35 U.S.C. 102(E) AS ANTICIPATED BY TIMM;

Claims 1,3-4, 12 and 15 were rejected under 35 U.S.C. 102(e) as being anticipated by Timm et al. (U.S. 6,055,268).

The Examiner has cited the Timm reference as teaching "at least one row and column transform circuit coupled to the input sample delivery circuit to effect a pipelined 2-dimensional FT of each sample array ..... dynamically reconfigured for each successive

sample array ..." and has cited col 3 lines 12-18 and col. 6 lines 11-18 of the Timm reference in support of same. (Office Action of December 18, 2003 at page 6).

The Applicant respectfully rejects the Examiner's characterization of the Timm reference. No where in the cited sections is any more than a cursory reference to a Fourier Transform made: "*The modulation of the coded bits is performed ...by using a 512-point ... fast Fourier transform* " (Timm at Col. 3, line 12-14). There is no teaching in the Timm reference as to any particular apparatus or method of computing a Fourier Transform, which is by contrast specifically the subject matter of the Applicant's invention. As the Examiner is well aware the use of an FFT for modulating and demodulating digital multi-tone communications is a requirement of the standard.

The only specificity in the cited sections of the Timm reference appears in the teaching of what is known as a fixed point, e.g. 512-point, FFT. This teaching it is directly opposite to the Applicant's teaching in which the size of the two-dimensional Fourier transform is dynamically configurable to correspond with the particular DMT protocol, and the number of tones or sub-carriers specified thereby.

Finally, and most troubling to the Applicant, the Examiner appears to rely on the Timm reference also for teaching a dynamically reconfigurable FFT and cites col 6, lines 11-18 in support of same. (Office Action of December 18, 2003 at page 6.) The cited section of the Timm reference reads as follows: "*A new rate negotiation method of the present invention enables a variable-rate DSL ... system. Using the rate negotiation method, the variable rate system adapts its throughput based on line conditions, ...This service can be added to a telephone subscriber loop without disrupting the plain old telephone service...*"(Tim at col. 6, lines 11-18, Emphasis). The cited section appears to deal with a single DSL subscriber line and the ability to vary transmission rates on same by varying bit loading on each tone as indicated elsewhere in the Timm specification. "*Discrete multi-tone (DMT) modulation transmits low-rate symbols over parallel subchannels. ...Good portions of the overall bandwidth (those subbands with high signal-to-noise ratio ...are used to transmit symbols with a larger number of bits/symbol. An unequal number of bits are assigned to different subchannels, depending on the available capacity of each subchannel.* " (Timm at Col. 24 lines 61-67, Col. 25, lines 1-3).

The Applicant respectfully submits that variable bit loading on the subchannels of a given DMT modulated subscriber line has nothing to do with the FFT itself, neither suggests implies, assumes, or requires any dynamic configurability of the FFT itself, and takes place outside of the FFT in modules such as the tone orderer and encoder in which the number of bits per symbol is determined. "*The tone orderer supports varying number of tones, bytes per tone and gain per tone for each of the X-DSL protocols. For example the number of tones for G.Lite is 128, for ADSL is 256 and for VDSL 2048. The number of bits to be extracted per tone is read from the tone-ordering table or register at the initiation of processing of each packet.*" (Applicant's specification at page 13, lines 9-12).

Applicant has amended all rejected Claims to include limitations related to a novel two-dimensional Fourier transform set forth as apparatus in Independent Claim 1 and Claims dependent thereon, and as process in Independent Claim 12 as follows:

- "*.....a two-dimensional Fourier transform circuit coupled between the input and output memory to perform the corresponding transformation of the input sample set and having:*
    - *row transform components including a Radix-R butterfly having "R" inputs and "R" output nodes; and the row transform components generating partial row transforms limited to solutions to a single unsolved one of the "R" output nodes of the Radix-R butterfly on each of the "R" iterations through ordered sets of samples from each input sample set; and*
    - *column transform components coupled to the row transform components and configured to generate complete column transforms from the partial row transforms generated by the row transform components prior to a completion of the "R" iterations through each input sample set by the row transform components; thereby to reduce an interval required to transform each successive input sample set.*" (Applicant's amended Claim 1)

- "*....generating partial row transforms limited to solutions to a single unsolved one of the "R" output nodes of the Radix-R butterfly on each of "R" iterations through ordered sets of samples from each input sample set stored in the storing act; and*

- *generating complete column transforms from the partial row transforms generated in the first generating act prior to a completion of the "R" iterations through each input sample set in the first generating act; thereby to reduce an interval required to transform each successive input sample set from a corresponding one of a time-to-frequency domain and a frequency-to-time domain.*" (Applicant's amended Claim 12)

The Timm reference neither discloses or teaches the Applicants novel two-dimensional Fourier transform circuit the components of which are the subject of Independent Claim 1, and the processes of which are the subject of the remaining Independent Claim 12. The Applicant therefore submits that the Timm reference does not anticipate either amended Claim 1 or Claim 12, and that the rejections of these Claims be withdrawn and that they be allowed. Remaining amended Claims depend either directly or indirectly from a corresponding one of Claims 1 and 12 and are for the reasons discussed above and for other reasons of independent significance also believed to have been placed in a condition for allowance.

10-11. CLAIMS 2 AND 13-14 REJECTED UNDER 35 U.S.C. 103(A) AS BEING OBVIOUS OVER TIMM, IN VIEW OF ALI;

Claims 2 and 13-14 were rejected under 35 U.S.C. 103(a) as being obvious over Timm et al. (U.S. 6,055,268), in view of Ali (Decimation-in-Time-Frequency FFT Algorithm").

Applicant has cancelled Claims 2 and 13. Claim 14 has been amended and no longer includes the rejected subject matter.

12. CLAIMS 5-6, 9-10, AND 18-19 REJECTED UNDER 35 U.S.C. 103(A) AS OBVIOUS OVER TIMM IN VIEW OF GOSSETT;

Claims 5-6, 9-10, and 18-19 are rejected under 35 U.S.C. 103(a) as being obvious over Timm et al. (U.S. 6,055,268) in view of Gossett et al. (U.S. 6,230,177);

The Examiner has cited the Gossett et al. reference as disclosing: "... *a 2-dimension FFT ...with...a row and column transform ...and at least one sliced radix circuit ...and at least one sliced radix circuit transforming 1/R input samples...into a selected one among the R possible complex outputs...and at least one variable order radix sub-module responsive to the input of each sample array to vary an order of the radix based on the dimensions of the sample array.*" (Office Action of December 18, 2003 at page 9 referencing Gossett et al. FIGS. 1, 4, 12 and the Specification at col 2, lines 60-65, and col. 5 lines 39-46).

Applicant has amended all rejected Claims. The Applicant does not share the Examiner's opinion as to the obviousness of or motivation for combining this reference with the Timm reference, irrespective of any FFT teachings therein. The Gossett reference has to do with image processing, specifically the use of FFT to perform texturizing in a graphics processing device, and offers no teaching on DSL or other subscriber line modulation and demodulation techniques. The Gossett reference lacks any structural detail beyond that associated with a graphics processing engine. The Gossett reference has the stated objective of performing FTs on existing graphics hardware. "*The remaining subsections of this section of the specification will set forth more details regarding the texture subsystem, how the computation of the FTs can be mapped to such a texture subsystem and how addressing techniques available in the subsystem can be used to select different types of FT computations, e.g. , a one dimensional FFT array, a vector radix 2x2 and others.*" (Gossett et al. at col. 8, lines 29-36).

Assuming, argued, that the appearance of a Radix-4 butterfly in the Gossett teachings was enough to produce motivation or obviousness to combine with the Timm reference, it would still be the case that there is no similarity in the FTE components set forth in the Applicant's amended Claims and the texture subsystem of the graphics hardware disclosed by Gossett. Specifically, no similarity in the point of integration of a Radix-R component or the functioning thereof, between the Applicants FTE and that disclosed by Gossett.

In view of the amendments to the Claims, and the remarks above, the Applicant respectfully submits that the rejections based on the combination of the Gossett et al. and Timm references have been overcome and that they be withdrawn.

13. OBJECTIONS UNDER 35 U.S.C. 132 TO THE AMENDMENT AS ADDING NEW MATTER:

Objections under 35 U.S.C. 132 to the amendment as adding new matter into the original disclosure.

The Examiner's rejections under this section believed to be have been overcome both by virtue of amendments to the Claims as well as by the Applicant's remarks with respect to both the Drawing objections under 35 CFR 1.83(a) and the written description rejections under 35 USC 112 1st paragraph.

The Applicant therefore, respectfully requests that these objections be withdrawn.

AMENDED CLAIMS SUPPORTED IN DRAWINGS AND SPECIFICATION:

The Applicant has amended all Claims support for which amendments is found throughout the specification, no new subject matter has been added. Independent Claim 1 is presented without markup and with annotations referencing at least some of the corresponding portion(s) of the drawings in which support for their subject matter is found. Next to each drawing is a reference number to assist the Examiner in locating the relevant portion of the specification in which a description is found. :

Claim 1 *"An apparatus for processing input sample sets of at least one discrete multi-tone (DMT) modulated communication channel, and the apparatus comprising:*

- *an input memory storing each input sample set as a two-dimensional array of rows and columns of samples;* ***(FIG. 4: 416-418; FIG. 9A:800; FIG. 9B:850; FIG. 10: 800,; 1020-1026;FIG. 11C, FIG. 12A:800; FIG. 12B:850; FIG13A-D:416-418; FIG. 16:1602;)***

- *an output memory storing two-dimensional arrays of rows and columns of coefficients resulting from a corresponding one of a time-to-frequency domain transformation and a frequency-to-time domain transformation of each input sample set;* ***(FIG. 4: 410-412; FIG. 9A:804; FIG. 9B:854; FIG. 11C; FIG. 12A:804; FIG. 12B:854; FIG13A-D:412-410;FIG. 16:1628,1668;)*** *and*

- *a two-dimensional Fourier transform circuit coupled between the input and output memory to perform the corresponding transformation of the input sample set and having:* ***(FIG. 4: 414;FIGS. 13A-D 414, 414A-D; FIG. 16: 1600-1676;)***

    - *row transform components including a Radix-R butterfly having "R" inputs and "R" output nodes; and the row transform components generating partial row transforms limited to solutions to a single unsolved one of the "R" output nodes of the Radix-R butterfly on each of the "R" iterations through ordered sets of samples from each input sample set; and* ***(FIG. 4: 414; FIG. 9A-B: 810,860;FIG. 10: 1000; FIG. 11C; FIG. 12A:1202-1210; FIG. 12B:1252-1260; FIG. 13A-D: 1300-1310, 1312-1324;FIG. 14A-B: 1300-1302, 1400-1450;FIG. 15: 1312, 1500-1520;FIG. 16: 1648-1662, 1670-1674, 1608-1624, 1630-1634)***

    - *column transform components coupled to the row transform components and configured to generate complete column transforms from the partial row transforms generated by the row transform components prior to a completion of the "R" iterations through each input sample set by the row transform components; thereby to reduce an interval required to transform each successive input sample set."* ***(FIG. 4: 414; FIG. 9A-B: 814,864; FIG. 11C; FIG. 12A:1212-1214; FIG. 12B:1262-1264; FIG. 13A-D: 1330-1384; FIG. 15; FIG. 16: 1664-1668, 1626)*** (Applicant's amended Claim 1 without Markup)

NEW CLAIMS

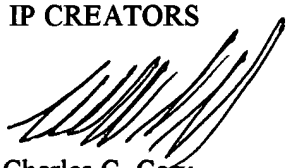
Applicant has added New Claims 22-23, support for which is found throughout the specification.

CONCLUSION

In view of the above remarks, and the amendments to the Claims, Applicant believes that all remaining Claims 1, 3, 5-10, 12, 14, 16-19 as well as new Claims 22-23 have been placed in a condition for allowance, and requests that they be allowed. Early notice to this effect is solicited.

The Commissioner is authorized to charge any additional fees which may be required, including petition fees and extension of time fees, to Deposit Account No. 50-1338 (Docket No. **VELCP003**).

Respectfully submitted,
IP CREATORS



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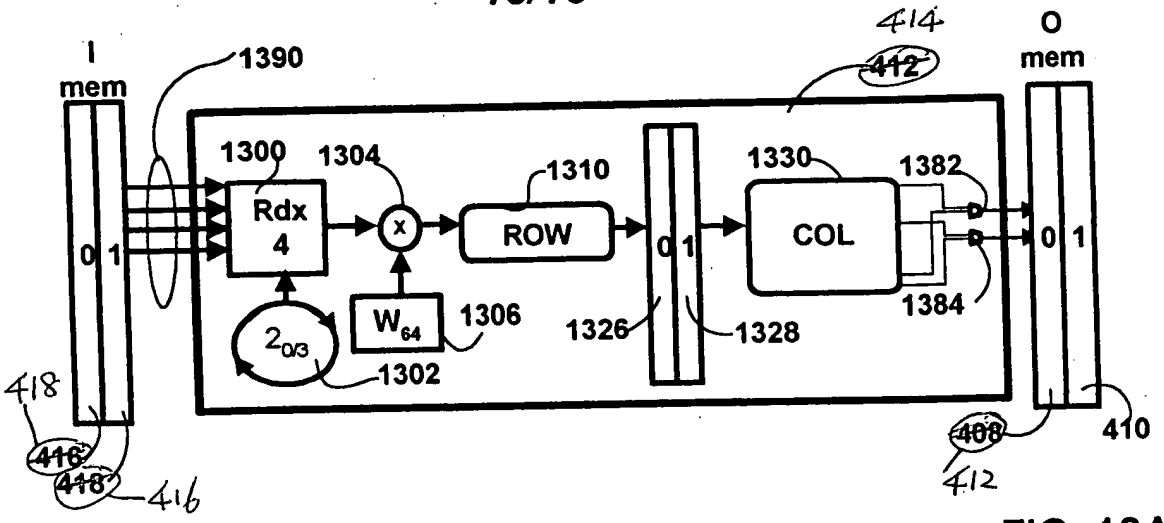


FIG. 13A

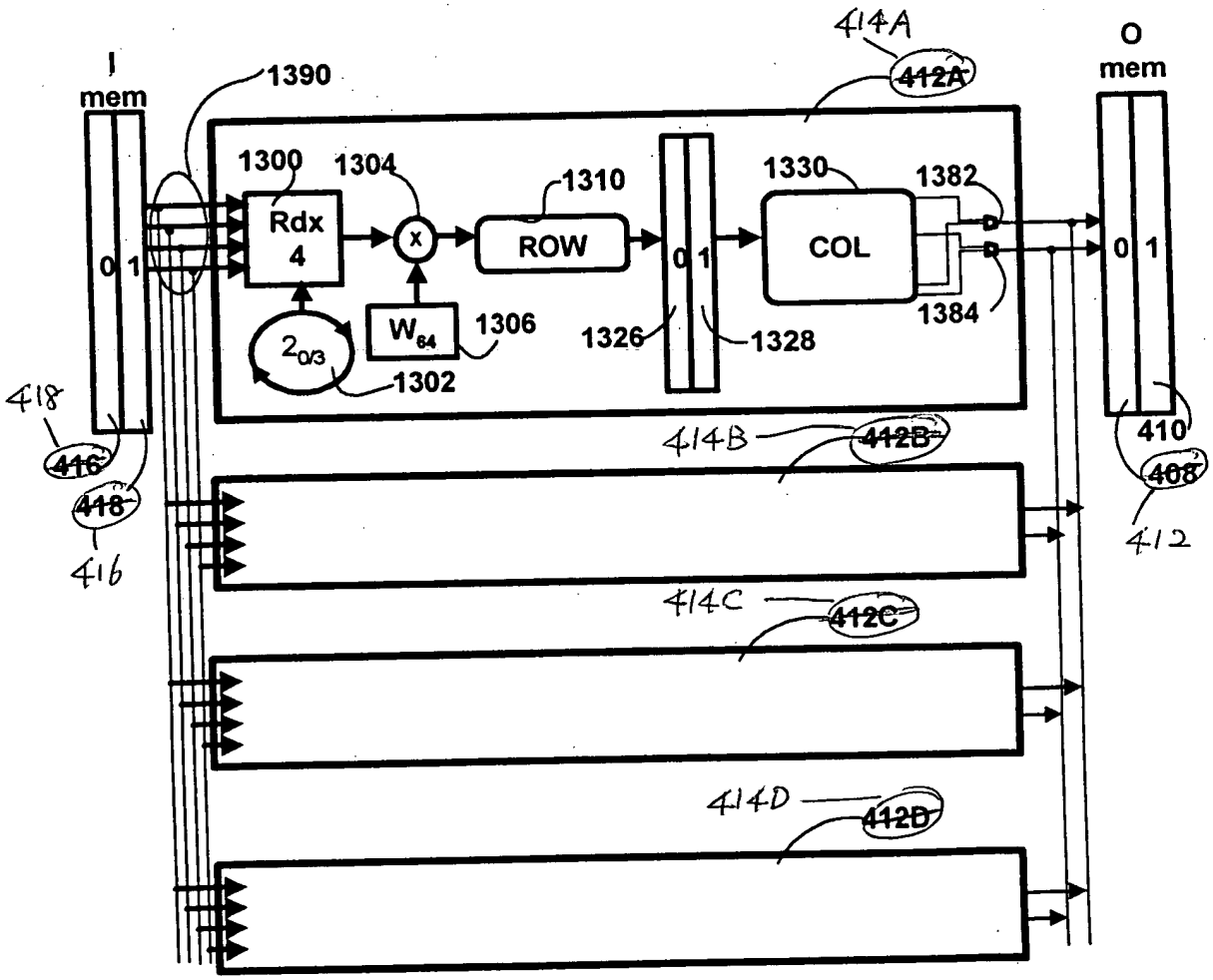
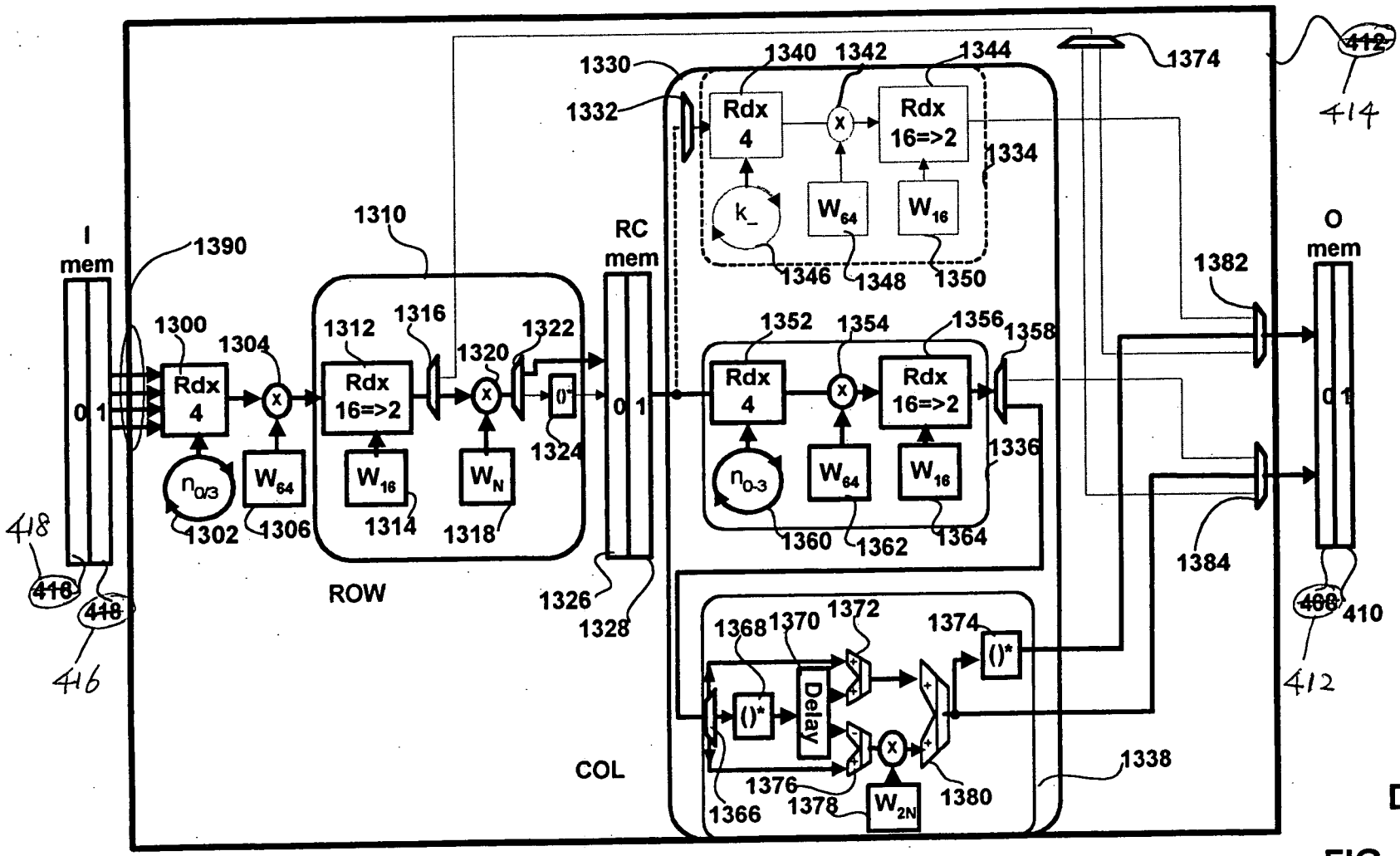


FIG. 13B



DFT

FIG. 13C

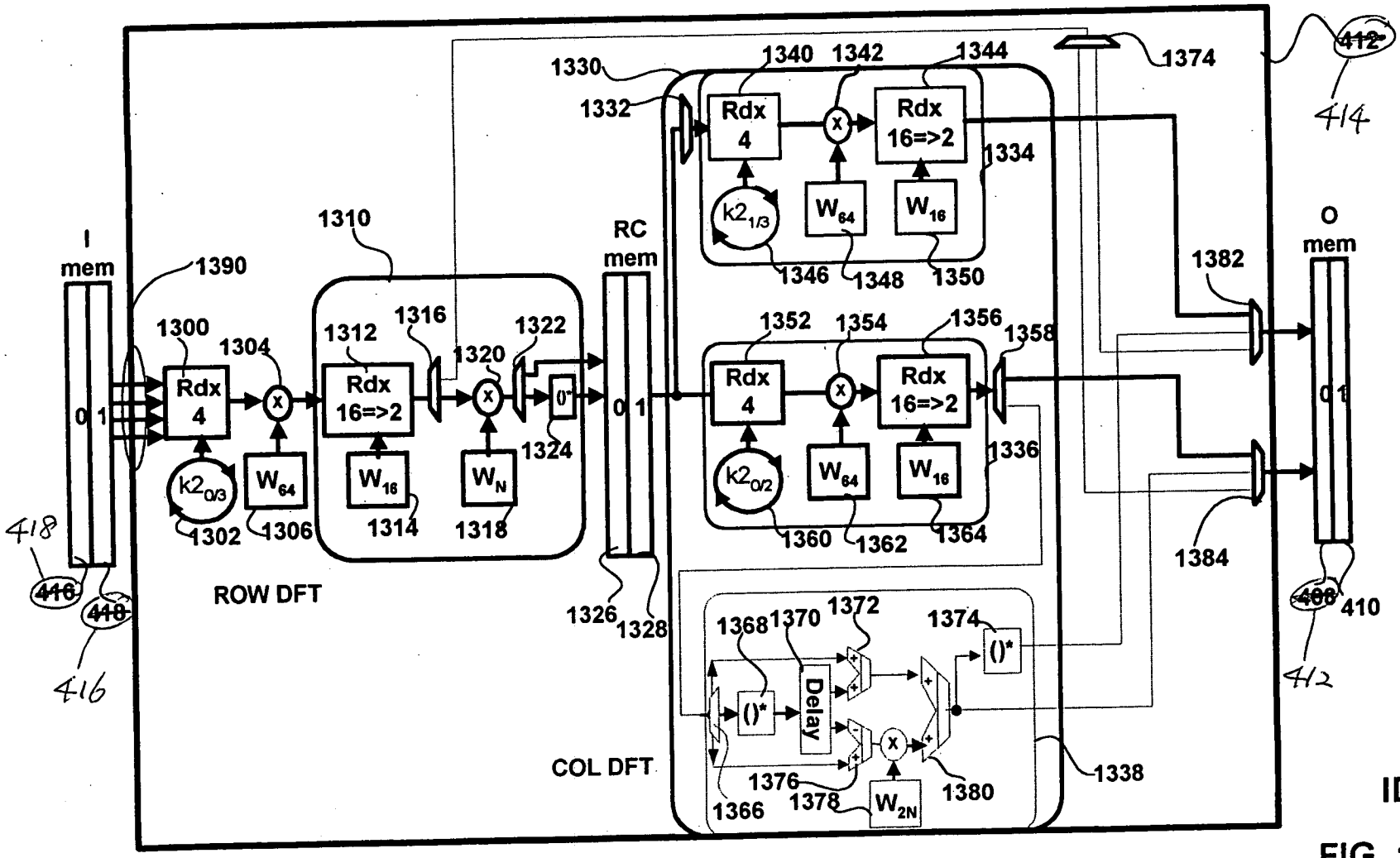


FIG. 13D